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Design and Implementation of QPSK Modulator Using FPGA Based on DDS algorithm

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Abstract

Digital modulators have become a hot research topic because of the progress in Radio Frequency (RF) front end terminals and systems on chip industry. But with all the progress that has been made, the implementation cost is still a challenge. This research paper presents a new architecture of construction Quadrature Phase Shift Keying (QPSK) modulator in VHDL at the lowest possible implementation cost. Four different carrier signals were generated using two 8-bit accumulators and 64 values Look Up Table (LUT) depending on the concept of Direct Digital Synthesizer (DDS) technique. The first accumulator operates on the rising edge of the clock, while the second one operates on the falling edge of the clock. The most significant bit in each accumulator was reversed using the XOR logic function. This process represents generating out-of-phase signals (180-degree phase difference compared with the original ones). The whole implementation process was done directly in Very high speed integrated circuit Hardware Descriptive Language (VHDL) using XILINX Vivado without the assistance of any co- simulation tool like DSP Builder Tools or Xilinx System Generator. The presented fulfillment technique based on the 64 values LUT has reduced the utilization resources by more than 70%.

Keywords—DDS, Digital Modulators, Look Up Table, LUT, VHDL

1 Introduction

Software Defined Radio (SDR) was introduced by Mitola in the 1990s as a technique to implement radio transceivers(Mitola, 1993, 1995, 1999). It has dominated the space for building various communication systems. It offers a high degree of flexibility as compared to the hardware-based systems. The construction of any SDR-based system is directly dependent on the availability of hardware peripherals(Wei, Zong, & Sun, 2023). These hardware peripherals act as the main parts in SDR based systems. One of the most commonly used terminals in an SDR based system is the Universal Software Radio Peripherals (USRP). The USRP consists of Field Programmable Gate Array (FPGA), DAC(Digital to Analog Converter),ADC (Analog to Digital Converter), and mixers. FPGA does most of the processing tasks. The progress that has been seen recently in the system-on-chip (SoC) industry is is supposed to reduce the implementation costs of building SDR systems. Unfortunately, the implementation cost still high especially for simple carry-on- radio transceivers.

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The higher cost comes from either the used hardware terminals or the used implementation software. To reduce this cost, many scholars have been seeking substitutes and alternatives. Almost all of the proposed solutions have concentrated on the use of ASIC, Applied Specific Integrated Circuits, or FPGAs as in addition to other electronic parts to use as a replacement of the USRPs. They used higher level co-simulation tools such as Xilinx Systems Generators or DSP Builders Tools as the main realization software.

The authors in (Quadri & Tete, 2013; Al Safi & Bazuin, 2016, 2017) summarized the most important work that has been done in this direction. Different modulation schemes have been investigated from simple ones such as ASK, Amplitude Shift Keying, FSK, Frequency Shift Keying, and PSK, Phase Shift Keying(Bhore & Sarde, 2014; Erdoğan, Myderrizi, & Minaei, 2012; Popescu, Gontean, & Budura, 2012; Chye, Ain, & Zawawi, 2009)and even some complex schemes such as QAM, Quadrature Amplitude Modulation and QPSK, Quadrature Phase Shift Keying (Song & Yao, 2010; Kazaz, Kulin, & Hadzialic, 2013; Elamary, Chester, & Neasham, 2009). Some researchers have gone even beyond this goal and have been trying to extend the conceptualization of SDR to implement what is called an "all-digital transmitter"(Ye, Grosspietsch, & Memik, 2007), where the binary formatted Radio Frequency (RF) signal can be directly synthesized in digital domain without going from/back to analog domain. PWM, Pulse Width Modulation, is very suitable for achieving that goal via Very high speed integrated circuit Hardware Descriptive Language (VHDL) using FPGA since it needs a low rate signal processing. A lot of progress has been done so far but we still need to do more such as reducing the hardware implementation cost and using affordable software (Jothimani, Narmadha, Santhiya, & Priya, 2023; Seelam, Prusty, et al., 2024; Wei et al., 2023).
This research present a new architecture of implementing QPSK modulator on FPGA board using 64 values Look Up Table (LUT) at the lowest possible utilization resources. Up to our knowledge, no such work has been proposed or used this trick before in terms of FPGA based digital modulators. The rest of the research is organized as follow: Section 2 illustrates the proposed implementation method, Section 3 illustrates the theoretical background of QPSK, Section 4 describes in details the implementation procedure, Section 5 discusses the obtained results, and finally section 6 is the conclusion and recommendation for future work.

2 Proposed Methodology

Generating the carrier signal plays a crucial rule in the implementation of any digital modulators since it represents the main part in all of the modulator systems. There are two common methods of generating the carrier signal in digital systems. The first one is COrdinate Rotation DIgital Computer (CORDIC) which is also named Volder's algorithm (Adiono, Ahmadi, Renardy, Fadila, & Shidqi, 2015; Urs, Aravind, Veni, & Yashwanth, 2023). The second one is based on Direct Digital Synthesis (DDS) algorithm(Misono, Namba, & Sumantyo, 2023) using LUT(Al-Safi & Alhafadhi, 2018). The concept of the second method is a little easier than the first one however the generated waveform is not very smooth like the CORDIC based one. Hence we used the LUT method since our main goal is to keep the utilization resources at low level. To generate a sinusoidal signal based on the LUT method, we need two components i.e phase accumulator and phase to signal waveform converter. The phase accumulator represents the angles which vary from 0-360 degrees while the phase to waveform converter contains the amplitude of the sine or cosine at that angle (represented by the accumulator). The sine and cosine signals amplitudes change in a certain way as the angle is changing but there is a relation between the amplitudes as we move from one point to another. So instead of saving a full period of the signal that we need to generate, 25%, which is from 1 to 128 time sample, might be enough to generate the rest of the signal as shown Figure 1.

3 Theoretical Background

QPSK has the constellation diagram shown in Figure 2. There are four points on the constellation diagram representing QPSK symbols. The bock diagram of QPSK modulator is shown in Figure 3. As the Figure illustrates, the binary incoming message need to be reformatted from serial version to parallel version, where some of the incoming bits have to be modulated using cosine carrier while the others are going to be modulated using sine carrier before they get summed together to construct the QPSK modulated symbol. The general QPSK symbol is(Al Safi & Bazuin, 2016):

$$s_n(t) = \sqrt{\frac{2E_s}{T_s}} cos(2\pi f_c t + (2n-1) * \frac{\pi}{4}) \quad (1)$$

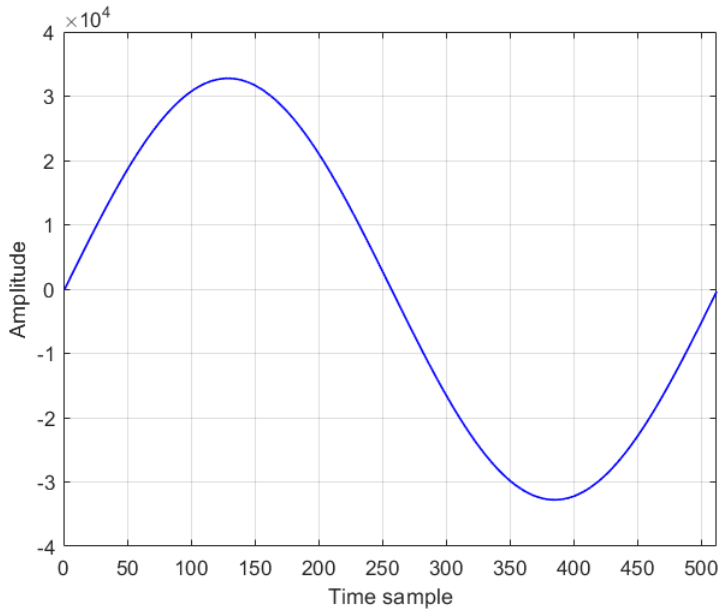


Figure 1: Full Wave sine signal.

Where E_s and T_s are the symbol energy and duration respectively, and fc represents the carrier frequency. As it shown in (1), four distinct signals can be get depending on the value of n. There is a phase difference of 90-degree between these signals. The phase difference comes from ((2n-1) /4), so as n is changing, this part of equation 1 will give as different angles. So, this means it is possible to generate QPSK modulated signal using four carriers with 90-degree phase shift. This concept is also known as Feher modulation scheme(Law & Feher, 1997).

4 Implementation details

We used the concept of Feher modulation scheme(Law & Feher, 1997)to generate the QPSK modulated signal. The block diagram of the implemented modulator using VHDL is illustrated in Figure 4. To generate the carrier signals, we used two 8-bit accumulators. The first one is working on the clock's rising edge whereas the second one working on the clock's falling edge. These accumulators will cover 256 value from 0 (00000000) to 255 (11111111). Based on these accumulators, we can generate two signals. The other signals are generated utilizing exactly the same two accumulators after altering their most significant bit using XOR logic function(Al Safi & Bazuin, 2016)as shown in Figure 4. To get the amplitudes that corresponding to the phase represented by the accumulators, we used 64 values LUT instead of 256 values LUT as it was explained in the previous section. The least significant 6-bit of the accumulators, will be used to look within the 64 values LUT while the most 2-bit will be used to select the quarter location(00 means the first quarter,01 means the second quarter, 10 means the third quarter, and 11 means the fourth quarter). Based on the obtained value from the LUT and the quarter location, the carrier waves got generated. This process of carrier generation reduces the utilization resources by more than 70%.

5 Implementation results

The obtained results from following the implementation procedure illustrated in the last two sections using XILINX Vivado software are shown in Figure 5. It shows QPSK signals under different circumstances. We have to mention here that the message signal was assumed to be an arbitrary signal driven by the clock signal. It can also be replaced by any other signal format. The signals shown in Figure 5 are plotted in MATLAB after exporting the data from XILINX Vivado to MATLAB since MATLAB has better visualization tools. The width of the modulated signal is 8-bit. The 16 bit width will give a smoother signal, but the utilization resources might increase. To get a cleaner signal, certain filters must be used, which is beyond the scope of this paper. Our implementation method is different from others on the basis of the strategy

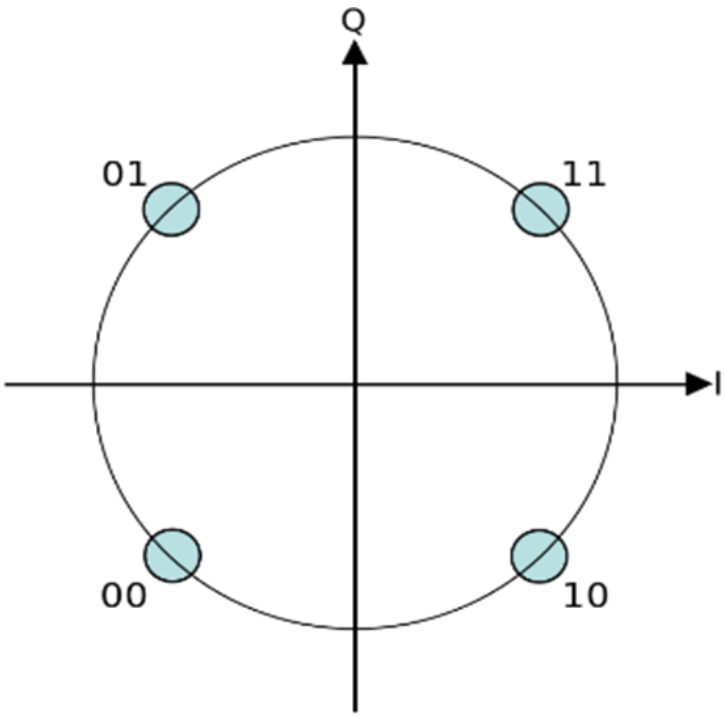


Figure 2: Constellation diagram of QPSK.

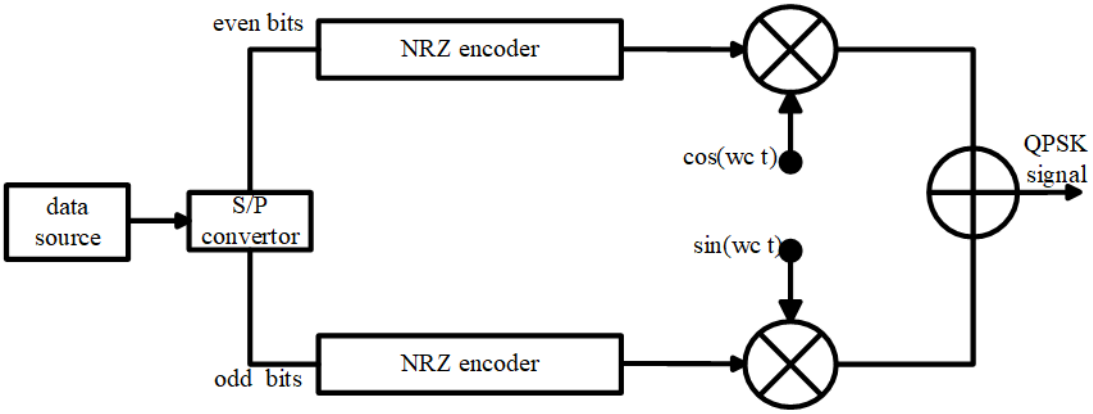


Figure 3: Block diagram of QPSK.

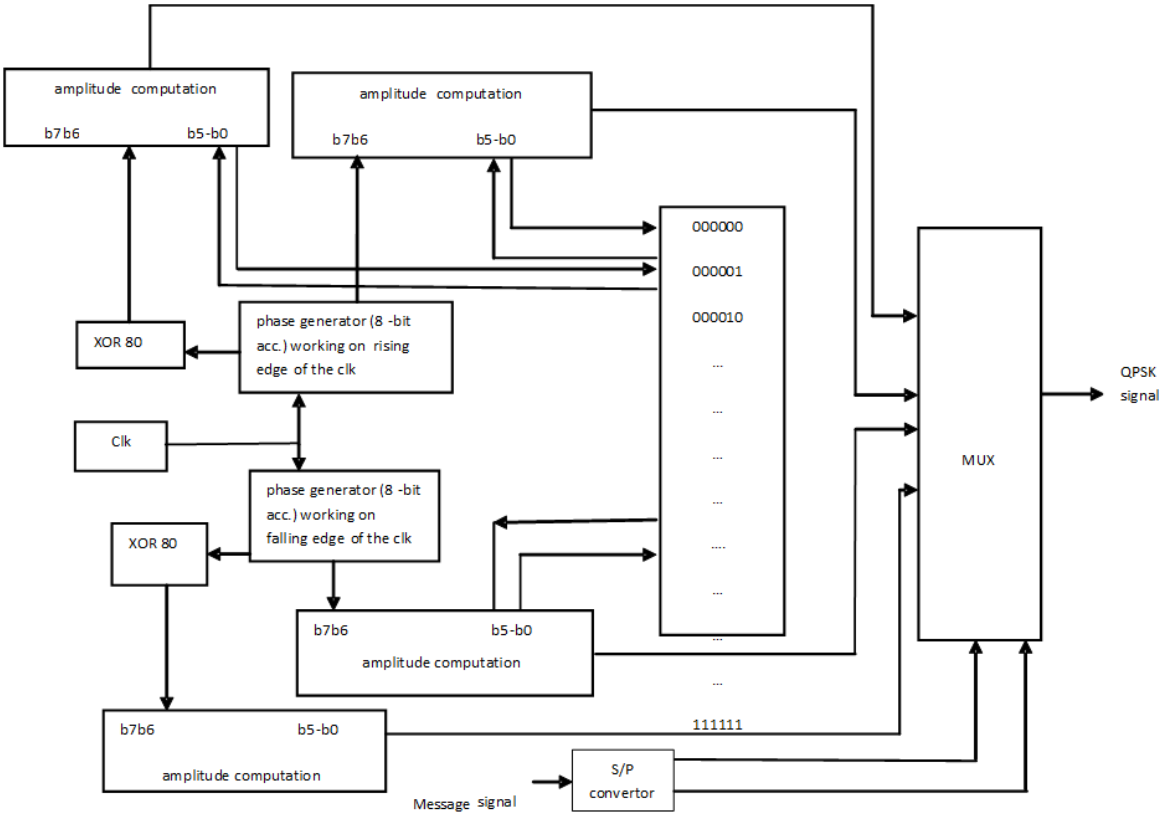


Figure 4: Implementation Schematic of the proposed system.

Table 1: Summary of the proposed method resources' expenses.

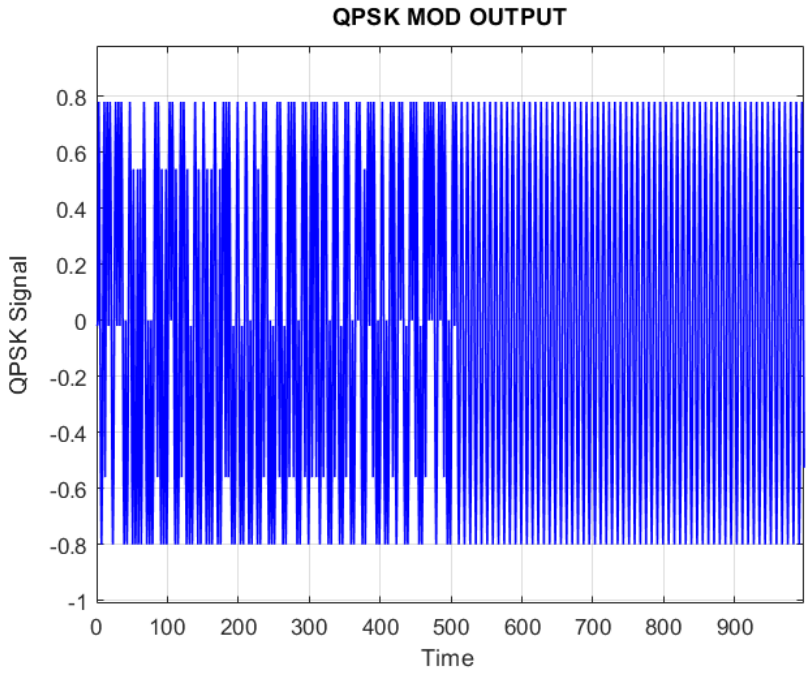
Resource	Utilized Resource	Total Available	Utilization percentage %
LUT	5	17600	0.03
FF	3	35200	0.01
IO	9	100	9
BUFG	1	32	3.13

used to generate carrier waves at various phase shifts and the tools used for that aim. We did not utilize any phase shifts as in(Elamary et al., 2009), MATLAB SIMULINK and System Generator as in (Song & Yao, 2010; Kolankar & Sakhare, 2014)or DSP Builder as in(Kazaz et al., 2013). It is also different from(Al Safi & Bazuin, 2016)based on the size of the LUT and how we compensate the size reduction to get a complete carrier signal.

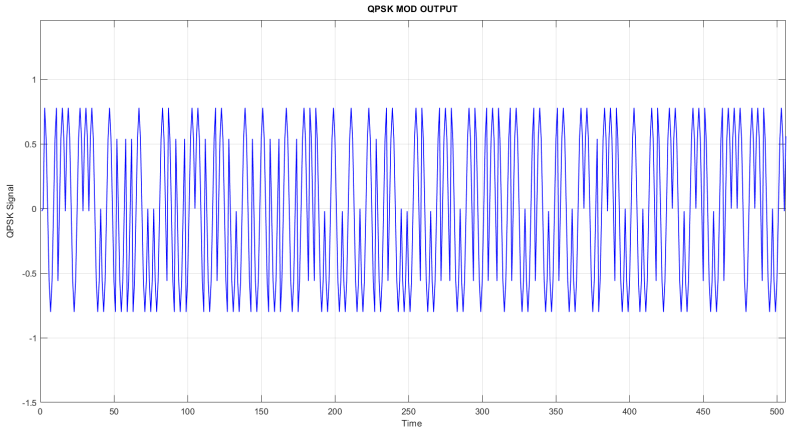
To justify our new design scheme, we download the design on ZYBO FPGA board. ZYBO board is an entry level board built around Zynq-7000 (Z-7010) family using programmable System-on-Chip (SoC) architecture.

After transferring the generated bit file to the intended board which was preceded by writing the .xdc file to allocate the appropriate inputs and outputs. The obtained resources consumption are shown in Table 1. Implementing the same QPSK modulator needed the utilization resources shown in Table 2 when a full wave based LUT was used. Now, the number of used slice LUT has reduced from 17 to 5, and the number of the used FF has reduced from 14 to 3. Hence, we reduced the required number of LUT by 71%, and the required number of FF by 79%. The other utilization resources stayed at the same usages.

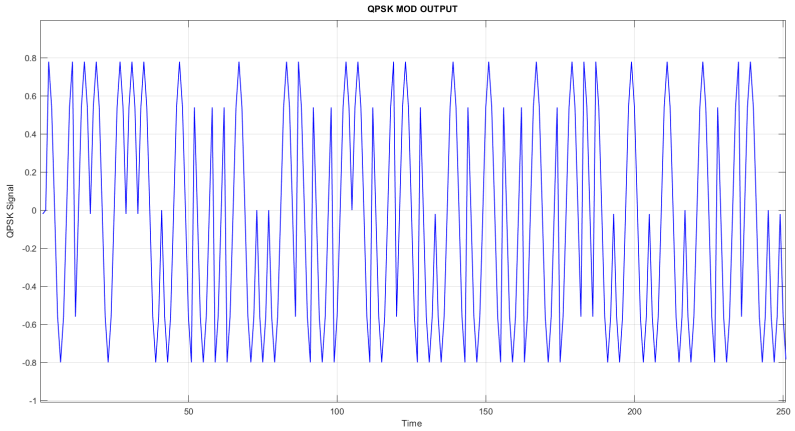
Compared with others' work(Al Safi & Bazuin, 2016), the proposed model used less Flip Flops and more Look Up Tables. In terms of costs and expenses, the proposed design costs less than others since it dosnt utilize any available IP cores or high co-simulation software(Elamary et al., 2009; Song & Yao, 2010; Kolankar & Sakhare, 2014; Kazaz et al., 2013).



(a)



(b)



(c)

Figure 5: QPSK modulation results in MATLAB at different zooming options(a-c).

Table 2: Summary of the resources' expenses presented in (Al Safi & Bazuin, 2016).

Resource	Utilized Resource	Total Available	Utilization percentage%
LUT	17	17600	0.1
FF	14	35200	0.04
IO	9	100	9
BUFG	1	32	3.13

6 Conclusion

This paper discussed a new method of utilization FPGA board to implement QPSK modulator. The implementation is based on, four sine signals generated based on 64 values LUT, two accumulator registers to compute the phase angle at different instances. The first accumulator is working on the clock's rising edge whereas the second one working on the the clock's falling edge. The most significant bit in each accumulator is reversed using XOR logic function and this process represent a 180-degree phase shift. After that, the four accumulated values (two within the accumulators and two after reversing the most significant bits) are used to generate four different carriers. The least significant six bits in each time aew used to obtained the corresponding amplitude of the sine signal while the two most bits were used to select the location of the phase value which has a direct impact on the amplitude computation. The whole implementation process is done directly in VHDL using XILINX Vivado without the help of any co-simulation tool such as DSP Builder or Xilinx System Generator. The presented implementation method has reduced the utilization resources significantly. Currently, the number of used slice LUT has reduced by 71% while the number of used FF has reduced by 79%. As a future work, the authors will investigate the possibility of using the reduced size LUT method to implement other modulation schemes such as multi-level PSK, and multi-level QAM modulators.

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