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Seven-Level Inverter Topology with Fewer Switching Components

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Abstract
This work proposed a 7-level Inverter structure with minimum power components and controlling with pulse width modulation (PWM) techniques. This topology has three times the greater capacity for voltage boosting. The aim of this study is achieved using a single voltage source, eight switches, two diodes, and two capacitors. Three times voltage boosting, a small number of switches, reduced voltage stress, and a self-balanced capacitor is the main characteristics of this topology. The selective harmonic elimination pulse width modulation SHE-PWM technique, which is based on genetic algorithm optimization, is also used to isolate or eliminate undesirable low-order harmonics of the output voltage. To demonstrate the aforementioned benefits, a simulation was performed using MATLAB SIMULINK, and the corresponding THD results were compared with various modulation indices.

Keywords: - Multilevel inverter, switched capacitors, PWM technique, Voltage boosting ability.

1. Introduction

In recent years, multilevel inverters **(MLIs)** as a feasible solution for high-efficiency electric power-electronic conversion systems.

The primary reasons for using MLIs in a wide range of applications, including motor drives and the use of Solar and wind energy sources, to name a few, are their intrinsic characteristics, such as reduced voltage stress on power electronic semiconductor switches, for switching in low frequency, the efficient output waveform, minimum filter requirement, etc**.[1].** The basic multilevel inverters MLIs are listed as 1-Diode-Clamped (DC-MLI) 2-Flying-capacitors (FC-MLI) 3-Cascaded H-bridge(CHB-MLI)**[2]** Additionally, CHB-MLI needs many isolated dc sources, whereas NPC-MLI and FLC-MLI still struggle with the balance of capacitor voltages. Although there are numerous variations of these fundamental MLIs, such as symmetric cascade H-bridge (S-CHB), asymmetric Cascade H-Bridge (A-CHB), hybrid Neutral point clamped(NPC) with Cascade H-bridge CHB, etc., The overall structure increases the complexity of control by involving a large number of components **[3].** The electrical energy produced by renewable energy sources, such as photovoltaic (PV) arrays and fuel cells, is mostly low dc voltage and must be converted to higher ac voltage. One of the common approaches is to pair a front-end conventional MLI with a back-end dc-dc boost converter **[4].** As an alternative, switched-capacitor multilevel inverters (SC-MLIs) have been thoroughly researched as a new approach strategy to dealing with the issues listed above. Here, a switched-capacitor-based multilevel boost inverter was introduced in **[5]** while having no inductive-load ability, it helps to build seven levels with fewer components than standard topologies. Although the main aim of SC-MLIs is buck-type devices, some systems that use solar photovoltaics, fuel cells, or electric car batteries need additional boosting circuits **[6].** Furthermore, by eliminating the requirement for an additional boosting circuit, The circuit is simpler as a result of the fundamental idea of connecting SCs in parallel or series with the input voltage source **[7]-[8].**

To construct a structure with as few components as possible, a variety of MLIs for more voltage levels have been described in the literature due to the advantages of the SC technique. Ten switches and four dc sources are used in a thirteen-level (13-L) inverter [9]. It is created in ML's kite structure in [10]. . another kite-type with switched capacitance-voltage (K-Type SC-MLIs) which needed fourteen semiconductor switches, four capacitors, and a single dc source is presented in **[11** According to the literature review, it is evident that attempting to increase the output level causes the circuit to become more complex. Implementation is more expensive. Consequently, numerous investigations were conducted in the literature that has a big impact on reducing the consumption of various elements including voltage sources, power semiconductors, and switched capacitors. This study described a seven-level SC-based inverter with a three-voltage boosting gain. The following are a few of this topology's advantages:

1. To produce seven levels of synthesized output voltage, only eight power switches and two diodes are needed (Vo).
2. It only needs two balanced switched capacitors, and no additional circuits, sensors, or complicated control techniques.
3. inherent ability to change the polarity.
4. In the proposed technology, there are eight switches in total, but only four of them are active at any given voltage level, which significantly lowers power switching losses.

Section 2 provides a detailed description of the circuit, operating modes for the proposed seven-level inverter, and

the developed pulse width modulation (PWM) scheme. In section 3, it was discussed how to optimize SHE-PWM using a genetic algorithm to implement it in the suggested topology. A thorough comparison with the current topology is presented in section 4 using various metrics. The findings are discussed in section 5. The conclusion is included in section 6.

2- Proposed 7-level inverter

2.1 Circuit Description:

The seven-level multilevel structure with a switched capacitor is shown in Fig. 1. It includes a single DC source, eight switches, two diodes ($\mathbf{D_1}$, $\mathbf{D_2}$), and two capacitors ($\mathbf{C_1}$, $\mathbf{C_2}$). There are four complementary switches ($\mathbf{S_1}$, $\mathbf{S_2}$, $\mathbf{S_3}$, and $\mathbf{S_4}$). **Van** represents the inverter's output as determined by the source voltage (**Vdc**).

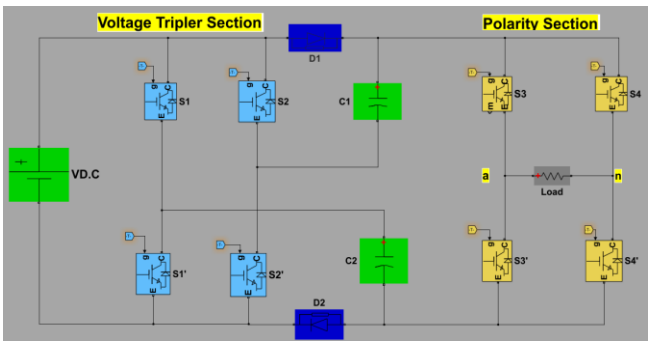


Fig.1 Proposed 7- level MLI structure

The topology here comprises two parts, The first part is a tripler part consisting of ($\mathbf{S_1}$, $\mathbf{S_2}$, $\mathbf{S_1'}$, $\mathbf{S_2'}$, $\mathbf{C_1}$, $\mathbf{C_2}$, $\mathbf{D_1}$, $\mathbf{D_2}$, and source voltage **Vdc**) of and is responsible for boosting the voltage to three times the input voltage, as shown on the left of Fig.1. The second is a polarity part is working together with the first part and contains four switches ($\mathbf{S_3}$, $\mathbf{S_3'}$, $\mathbf{S_4}$, and $\mathbf{S'_4}$, and **load**) to reverse the polarity of the part **(H-bridge)**.as shown on the right of Fig.1. If $\mathbf{C_1}$ and $\mathbf{C_2}$ are large enough just to keep a constant dc voltage without considering the forward voltage drop and on-state resistance of the switching devices and without the need for any closed-loop control, three different dc-bus voltages **(Vdc-bus)** can be produced. In other words, the series/parallel connection technique ensures the self-voltage balancing of SCs. Each component has experienced low voltage stress (**Vdc**). The proposed inverter is less complicated and more affordable because of this feature.

2.2 The Principle of Operation and SC Voltage Balancing:

The current flow path for a resistive load is shown in Fig. 2 following the switching states in Table I. The nine operating states in the suggested topology have been completed by
each cycle of operations. The switching table indicates the entry "**1**" for the ON state and "**0**" for the OFF state. to fully charge each capacitor ($\mathbf{C_1}$ and $\mathbf{C_2}$)to its maximum source voltage(Vdc) rating. the capacitors C1 and C2 are parallel connected to the source voltage in the voltage tripler section to $\mathbf{C_1}$ and $\mathbf{C_2}$ in charging operation. while capacitors discharged by connecting in series with the source Vdc, These two capacitors simultaneously discharged to the source and the load. in three voltage levels, self-voltage balancing of capacitors is ensured by connecting them in parallel for charging and in series to discharge. Capacitors $\mathbf{C_1}$ and $\mathbf{C_2}$ are connected in parallel with the Vdc during the voltage levels **±1Vdc**, therefore, as a result, charged at level **±1Vdc**. Depending on the selected switch state, either $\mathbf{C_1}$ or $\mathbf{C_2}$ discharges at voltage levels below **±2Vdc** while the other charges are, two capacitors in series with input source discharges, The operating modes are:

1-Vab=0V: During this state as shown in Fig 2 d, through the power semiconductor devices **($\mathbf{S_1'}$, $\mathbf{S_2}$ and $\mathbf{S_3'}$, $\mathbf{S_4'}$)** in the ON state position. the capacitors are not charged (idle), the canceling voltage across the load by ($\mathbf{S_3'}$, $\mathbf{S_4'}$). As a result, the load receives zero voltage.

2-Vab=Vdc: The state explains the capacitors $\mathbf{C_1}$ and $\mathbf{C_2}$ are simultaneously charged by the source voltage to produce load voltage(**Vdc**), with the power switches devices **(S1, S2', $\mathbf{S_3}$, and $\mathbf{S_4'}$)** in the ON state. In a similar manner, switches **($\mathbf{S_1}$, $\mathbf{S_2'}$, $\mathbf{S_3'}$, and $\mathbf{S_4}$)** are activated in a negative operation mode. The useful mode of operation is proved in Fig .2 a.

3-Vab=2Vdc: During this state, the load voltage **2Vdc** is obtained by switching ON the switches under Table I in states 2 and 3.

4-Vab=3Vdc: During this state 4, the input voltage to supply is coupled in series with the voltage storing devices capacitors $\mathbf{C_1}$ and $\mathbf{C_2}$, and the load voltage when **($\mathbf{S_2}$, $\mathbf{S_1'}$, $\mathbf{S_3}$, and $\mathbf{S_4'}$)**are ON so, the total gain of state 4 is **3Vdc** alternated.

Table 1 Switching states of a proposed 7-level inverter.

States	Tripler circuit		Polarity circuit		Capacitors		Van
1	1	0	1	0	charge	Charge	+Vdc
2	1	1	1	0	Discharge	charge	+2Vdc
3	0	0	1	0	charge	Discharge	+2Vdc
4	0	1	1	0	Discharge	Discharge	+3Vdc
5	0	1	0	0	Idle	Idle	0
6	1	0	0	1	charge	charge	-Vdc
7	0	0	0	1	Discharge	charge	-2Vdc
8	1	1	0	1	charge	Discharge	-2Vdc
9	0	1	0	1	Discharge	Discharge	-3Vdc

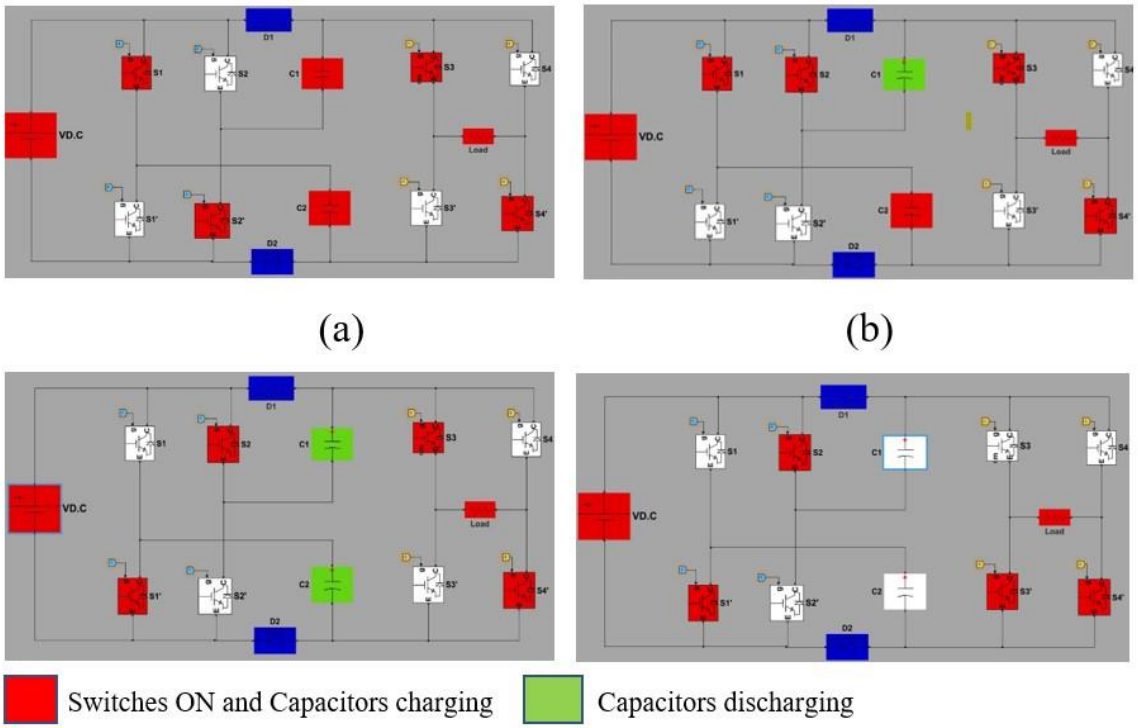
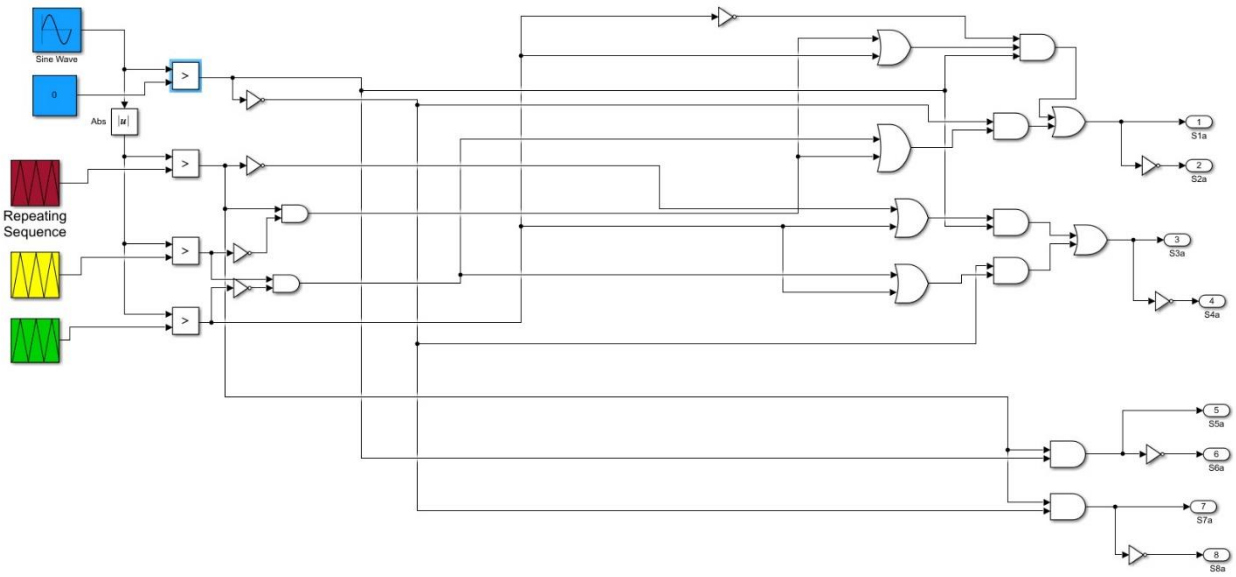
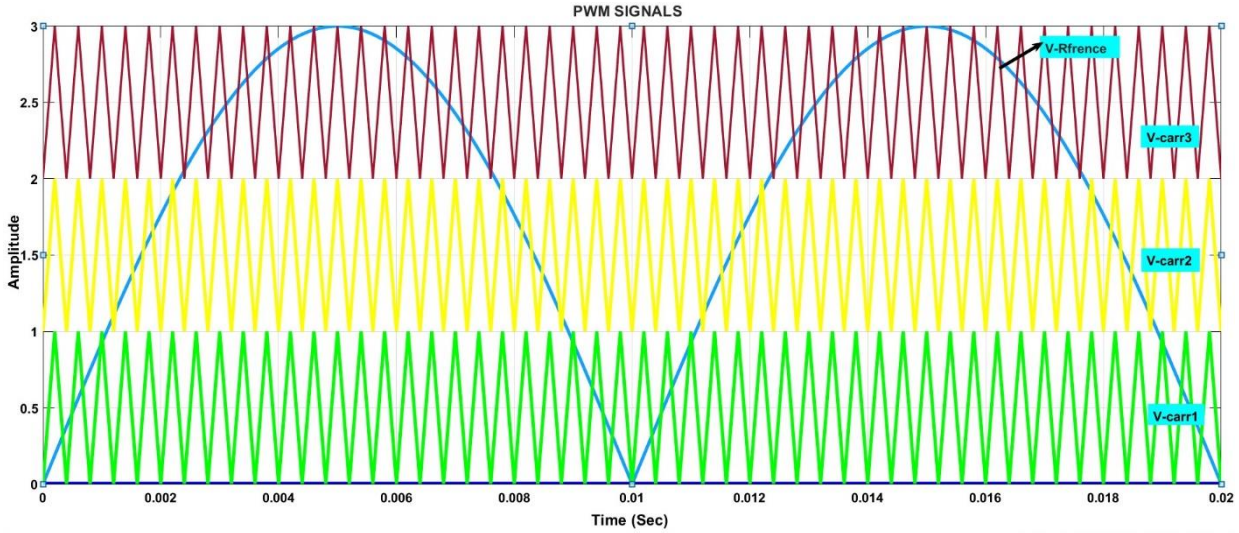


Fig.2 Modes of operation for 7-level MLIs with positive half-cycle and zero states. (a) stage 1 +1 Vdc.(b)Stage 2 = +2Vdc.(c)Stage= +3Vdc.(d) Stage 4 =0 V

2.3 PWM Strategy



(a)



(b)

Fig .3. Logic for PWM Signal Generation (a) Logic circuit ,(b) PWM

In multilevel inverters, the pulse width modulation (PWM) technique is used to control the switches ON and OFF states. To achieve this, improve the quality of the output voltage waveform and balance of capacitors voltage by reducing voltages ripples in it. the signal produced is in Fig.3 b by simple level shifted pulse modulation (PWM).three high-frequency triangular waveforms **(Vcarr1, Vcarr2, and Vcarr3)** are compared with a rectified sinusoidal reference **(Vref).**In the PWM technique, carrier signals **(Vcarr1, Vcarr2, and Vcarr3)** are shifted and in a similar phase. It is also working for higher and lower switching frequencies. the result of the comparator between reference signals and carrier signals is subjected to a suitable logic circuit[3]. which generates the level information for the output voltage to be produced as shown in Fig. 3. (a). For such an arrangement, the modulation index is given as:

$$Ma = \frac{Vref}{3\,Vcarr} \qquad (1)$$

where ***V-ref*** is the reference signal amplitude, and ***V-carr*** is the the triangular carrier signal amplitude**.** Only the switching state combination of switching states 2 and 8 with 3 and 7 will result in an equal power-sharing between the capacitors $\mathbf{C_1}$ and $\mathbf{C_2}$ because of the symmetrical charging and discharging. Thus, there will be no difference in the voltage ripple between them. The level indicator signals and Table I are used to create the gating signals. For example, if the selected combination of states is 2 and 8 with 1 and 6, Switch S2 must be turned ON for states 2 and 4 during the positive half cycle and 8 and 9 during the negative half cycle. The level outputs for these states are tapped, and the gating pulse signal is generated after the proper logic has been used. Similar progress is repeated to derive gating pulse signals for the switches' remaining modes.

2.4 Capacitor analysis

The states of operation listed in Table I was successfully arranged in one cycle of output voltage, taking into account
the staircase output voltage depicted in Figure 4, to balance the two capacitors. wherein $\boldsymbol{\alpha_1}$, $\boldsymbol{\alpha_2}$, and $\boldsymbol{\alpha_3}$ are conducting angles. $\mathbf{C_1}$ is used for double the voltage of **2Vdc** in the range of $\boldsymbol{\alpha_2}$ to α3 during the positive half cycle. **C2** is used for the voltage of 2Vdc from $\boldsymbol{\pi}$- $\boldsymbol{\alpha_3}$ to $\boldsymbol{\pi}$- $\boldsymbol{\alpha_2}$. And from α3 to $\boldsymbol{\pi}$- $\boldsymbol{\alpha_3}$ both C1 and C2 provide **3Vdc**. For the negative half cycle, a similar arrangement is also made. As a result, [14] is used to express voltage ripples across the two capacitors:

$$\Delta Vc1 = \frac{1}{2\pi f\, C1}\int_{\alpha 2}^{\pi-\alpha 3} io1\; d(wt)$$

$$\Delta Vc1 = \frac{1}{2\pi f\, C1}\int_{\alpha 2}^{\pi-\alpha 3} ic1\; d(wt) \qquad (2)$$

$$\Delta Vc2 = \frac{1}{2\pi f\, C2}\int_{\alpha 3}^{\pi-\alpha 2} io2\; d(wt)$$

$$\Delta Vc2 = \frac{1}{2\pi f\, C1}\int_{\alpha 3}^{\pi-\alpha 2} ic2\; d(wt) \qquad (3)$$

Where **io** is the output current of the inverter and ***f*** is the frequency of the output voltage.
The output current (io=Vo/R), io is inversely proportional to the Vo, when the load is used as a purely resistive R. The ripples of voltage can be described as:

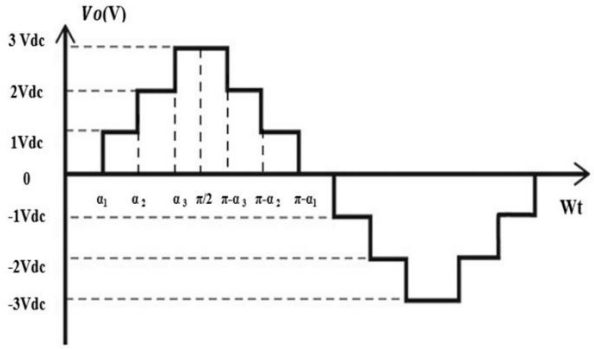


Fig .4. Operation describes how the 7-level inverter is configured for stair output.

$$\Delta VC1=\frac{(3\pi-4\alpha3-2\alpha2)Vdc}{2\pi fC1} \quad (4)$$

$$\Delta VC2=\frac{(3\pi-4\alpha3-2\alpha2)Vdc}{2\pi fC2} \quad (5)$$

It indicates that there is no difference in the voltage ripple between the two capacitors. Both capacitors operate twice, once in the positive half cycle and the negative half cycle alternately. the capacitor voltage ripple can be controlled by a suitable switching method.

3-Selective Harmonic Elimination technique

To eliminate the odd harmonics and control the fundamental voltage, the selective harmonic eliminated pulse width modulations (**SHE-PWM**) method is used to find the optimum switching angles, specifically **(α_1,α_2,…..,α_n).** The Fourier series can be used to express the output voltage (Vo) waveform mathematically[17]:

$$\mathbf{Vo} = \mathbf{ao} + \sum_{i=0}^{n} \mathbf{an}\cos[\frac{2\pi nf}{T}] + \mathbf{bn}\sin[\frac{2\pi nf}{T}] \quad (6)$$

For the symmetric staircase waveform with a quarter-wave, see Fig.4.The amplitude of the dc component equals zero (**a_0=0**), and The amplitude of all even harmonics equals zero (**bn=0**). the fundamental component's, **n=1**, and odd harmonic component's amplitudes are given by:

$$V_1=\left[\left(\frac{4Vdc}{\pi}\right)\sum_{K=1}\cos(\alpha k)\right] \quad (7)$$

$$Vn=\left[\left(\frac{4Vdc}{n\pi}\right)\sum_{K=1}\cos(n\alpha k)\right] \quad (8)$$

Where αk is the switching angles,n is odd harmonics, and the staircase waveform's switching angles will be adjustable to obtain the output voltage **THD** with the lowest possible. The total harmonic distortion **(THD**) is represented as follows:

$$\mathbf{THD}=\sqrt{\frac{\sum Vn\hat{}2}{V1\hat{}2}} \quad (9)$$

Five categories of finding three firings are included in the suggested topology to find the lower-order harmonics in the waveform angles of the output voltage waveform. The topology of a seven-level inverter,(**3rd,5th,7th,9th,11th**) odd harmonic is selected from the output voltage waveform for harmonic elimination. the firing angle (**α_1, α_2, α_3)** that was calculated using the constraint relationship **[0<α_1<α_2<α_3<π/2]** is calculated using equation (10):

$$\mathbf{V_n}=\frac{4V}{n\pi}[\cos(\alpha1)-\cos(\alpha2)-\cos(\alpha3)] \quad (10)$$

In the output voltage waveform, the 3rd harmonic (n=3), 7th harmonic (n=7), etc were eliminated[18].

$$\mathbf{V_1}=\frac{4V}{\pi}[\cos(\alpha1)-\cos(\alpha2)+\cos(\alpha3)]$$

$$\mathbf{V_3}=\frac{4V}{3\pi}[\cos(3\alpha1)-\cos(3\alpha2)+\cos(3\alpha3)]$$

$$\mathbf{V_5}=\frac{4V}{5\pi}[\cos(5\alpha1)-\cos(5\alpha2)+\cos(5\alpha3)]$$

$$\mathbf{V_7}=\frac{4V}{7\pi}[\cos(7\alpha1)-\cos(7\alpha2)+\cos(7\alpha3)] \quad (11)$$

$$\mathbf{V_9}=\frac{4V}{9\pi}[\cos(9\alpha1)-\cos(9\alpha2)+\cos(9\alpha3)]$$

$$\mathbf{V_{11}}=\frac{4V}{11\pi}[\cos(11\alpha1)-\cos(11\alpha2)+\cos(11\alpha3)]$$

To reduce the (3rd,5th,7th,9th, and 11th)harmonics in the output waveform, It has been set so that the corresponding voltage is zero. Utilizing the selective harmonic elimination technique, with the smallest number of switching and selecting the optimum firing angles, only particular harmonics are eliminated. This method is ideal for controlling inverters. This method makes it possible to obtain a low THD output waveform without the use of a filter circuit. Another method reduces THD by optimizing the switching angle using a genetic algorithm.

3.1 Genetic Algorithm(GA)

The goal is to determine the optimal switching angles that result in an output voltage with the required fundamental component and the fewest of THD that is logically possible. . An optimization algorithm should be used to resolve this issue. a genetic algorithm is used in this work. which is a simple, powerful, and evolutionary method inspired by the concepts of genetics and natural selection. It is a general-purpose stochastic global search algorithm that looks for solutions without considering functional derivative data. which reduces (or expands) a given objective function. While addressing complex objective functions, GA reduces computation and search time requirements [19]. The SHE-PWM technique's genetic algorithm is still an innovation. . To minimize the function ***f*** **(x_1,x_2,……,xk**)using **GA**. The first step is to encode each Xi as a length binary or floating-point string. A binary string, such as in the following:

X_1=[10011 …….11010]
X_2=[00111 …….11001]

↓

X_k=[11010 ……..…01101]

Where collective **{x_1,x_2,…..,x_k}** is called a chromosome, and xi is the genes.

3.2 Defining The Issue

Any application uses the same GA methodology. A GA only requires a small number of parameters to be set for it to function. The following are the procedures for formulating a problem and using the GA:

1- Choose between floating-point or binary strings.

2- Identify the variables that are important to the subject; this amount will stand in for the number of genes on a chromosome. The number of variables and the number of programmable switching angles is the same in this application. For a seven-level inverter, each chromosome will have three switching angles, or. (α1, α2, α3).

3- Define the population size and start it out. The higher population may speed up convergence but at the expense of longer execution times. When initializing the population with random angles between 0 and 90, consideration is given to the output voltage waveform's quarter-wave symmetry.

4- The cost function is the most crucial component in the GA evaluation of each chromosome's fitness. This study aims to reduce the output voltage's total harmonic distortion. In light of this, the cost function Fv is written as:

$$\mathbf{Fv}_{(\alpha_1,\alpha_2,\alpha_3)}=\sqrt{\frac{\sum_{n=3,5,7\ldots}(Vn)^2}{V1^2}} \qquad (12)$$

5-The GA is typically set up to run for a predetermined number of iterations in order to find a solution (20 in this case). FVs are used to identify new offspring after the initial iteration. These undergo crossover and mutation processes, and a new population is produced that follows the same cycle beginning with FV assessment. Sometimes, well before the 20 iterations are finished, the GA can converge to a solution. The answer must also meet the following fundamental constraint[20]:

$$[0<\alpha_1<\alpha_2<\alpha_3<\pi/2] \qquad (13)$$

4-Comparison with Other Recent SCMLI Topologies:

Parameters comparison with existing seven-level inverters is made in Table II. wherein **E** represents one level of the output voltage,(**Nswitches**(N_{SW}),**Nsource**(N_{SO}),**Ndiode**(N_D),**Ncapacitance**(N_C), and **N-level**(N_L)) represented the number of power semiconductor switches, DC source, and diodes, capacitors, and, output level inverter respectively.

Table 2 Parameters Comparision of 7-Level inverters

T	N_{SW}	Nso	N_C	N_D	N_L	TSV	C-Balance	Gain
[12]	7	3	3	2	7	15E	NO	1
[13]	16	1	3	0	7	16E	YES	3
[14]	16	1	2	0	7	16E	YES	3
[15]	10	2	3	0	7	16E	YES	1.5
[16]	6	3	3	8	7	14E	NO	1
P.w	8	1	2	2	7	16E	YES	3

The proposed 7-level inverter topology**(p.w)** is a symmetrical circuit comprised of a single DC source of **Vdc=100V**. For inverter configuration, the prime parameter is Total Standing Voltage **(TSV)**. It is the summation of the absolute voltage across every switching device, while the same voltage stress occurs in the complementary switch. Complementary switches,($\mathbf{S_1}$, $\mathbf{S_1}$')and ($\mathbf{S_2}$, $\mathbf{S_2}$'):

$$\mathbf{Vs_1 = Vs_1'} = \mathbf{Vs_1} = \mathbf{Vs_1'} = \mathbf{V_{dc}} \qquad (14)$$

Complementary switches, $\mathbf{S_3}$, $\mathbf{S_3}$' and $\mathbf{S_4}$, $\mathbf{S_4}$'

$$\mathbf{Vs_3 = Vs_3'} = \mathbf{Vs_4} = \mathbf{Vs_4'} = \mathbf{3V_{dc}} \qquad (15)$$

$$\mathbf{TSV}=\sum_{y=1}^{8} Vsy \qquad (16)$$

Therefore, substitute (14)– (15) in (16) yields:

TSV=16 Vdc

The **TSV** of **MLIs** is **16Vdc** and the **TSV p.u**. is computed by[21],

$$\mathbf{TSV\ p.u}=\frac{\mathbf{TSV}}{\mathbf{Vo,peak}}=\frac{16\,Vdc}{3Vdc}=\mathbf{5.333\ p.u} \qquad (17)$$

Where **Vo,peak** is the maximum output voltage**.**

$$\mathbf{The\ Voltage\ gain}=\frac{Vo.peak}{Vdc}=\frac{3}{1}=\mathbf{3} \qquad (18)$$

The work [16] uses the fewest switches overall but the most diodes compared to the works [13] and [14], which both use the most switches but no diodes. However, the total switch voltage (TSV) is essentially constant across all inverters. The works [12], [13], [15], and [16] all use three capacitors, whereas [14] and the proposed one only need two.

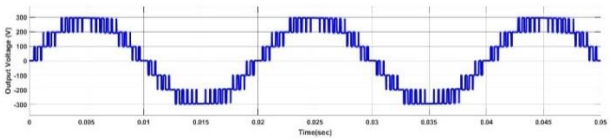
The three capacitors in [12] and [16] to divide the input voltage and maintain the balance of the voltage, are often connected in series. Therefore, to ensure capacitor voltage equalization, modulation techniques or additional balancing circuits are needed. In contrast, capacitors' voltage in [13], [14], can be connected in parallel multiple times during one cycle of output voltage with the input voltage source Vin, and the suggested one can be automatically balanced as a result. Additionally, as two H-bridges are formed by the eight power switches used in this proposed work, The proposed inverter benefits from a simpler design, step-up capability, and self-balancing capacitors voltages overall.

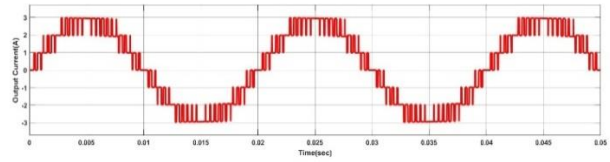
5-Results and Discussion

A less complicated and effective model has been constructed. It is investigated and assessed to show the significance and contribution of the suggestion inverter of seven levels in the **Matlab simulation program**. The requirements and elements are listed in TableIII and the source voltage is **100Vdc**. The PWM level shift is used to gating pulses control of the power semiconductor switches, wherein V-reference is equal **50Hz** and **V-carrier** is equal to **2.5 kHz**, and the ***Ma*** is set to **1**. A **2200 µF** capacitance was chosen for $\mathbf{C_1}$ and $\mathbf{C_2}$ respectively to minimize the capacitor ripple voltage. The resistive load of **100** ohms in the inverter and according to waveforms of output voltage, current.

Table 3 Simulation parameters of the proposed 7-l inverter

Description	Simulation
Source Voltage (Vin)	100 V
Load Voltage (Vo)	300 V
Carrier's frequency	2.5KHz
Fundamental frequency	50Hz
Switching frequency	2.5KHz
Capacitor (C1)	2200 µF
Capacitor (C2)	2200 µF
Load	100 ohms





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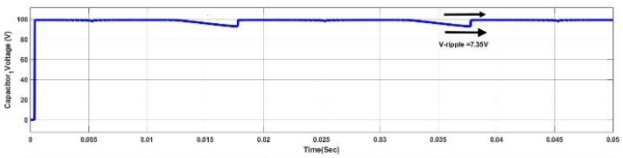
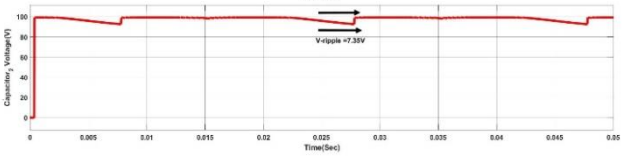
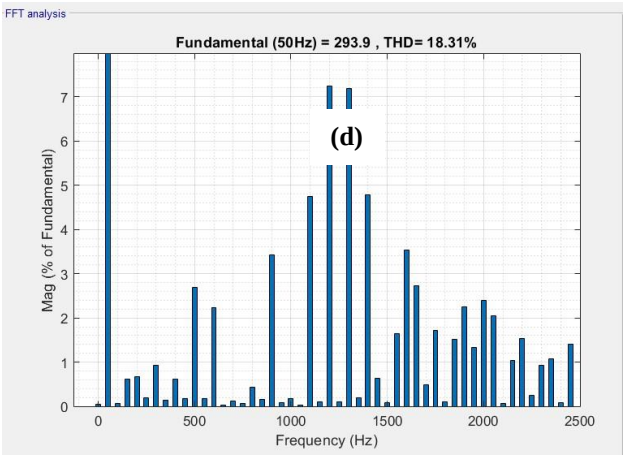
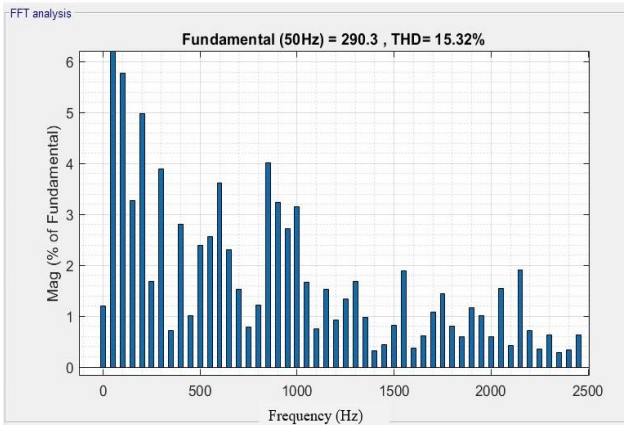






(d)



(c)

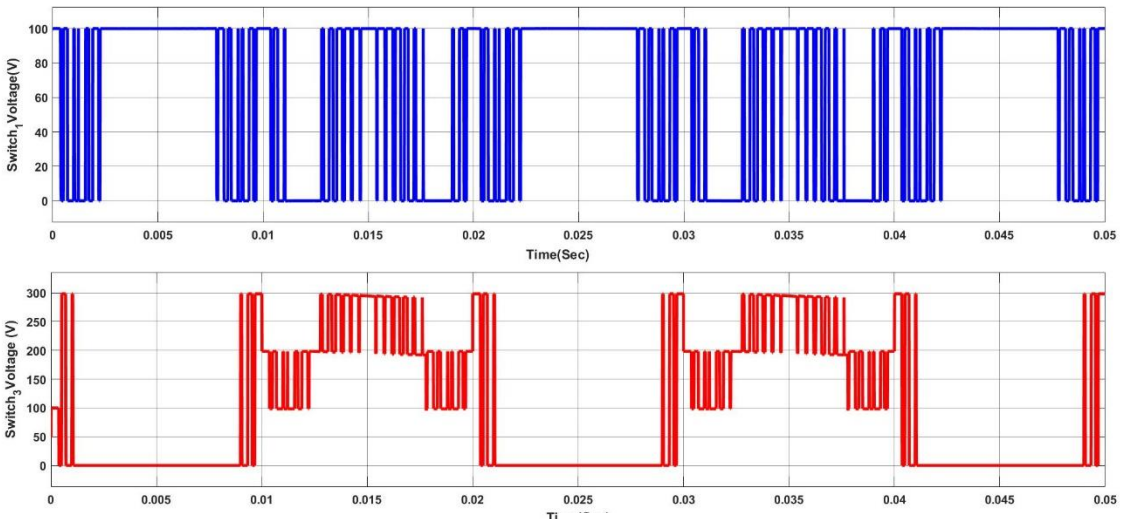


Fig. 5. Shows (a) Output voltage and load current with R load (b) capacitors Voltages (c),(d)Shows THD with GAs optimized firing angle for Ma =1 (e) Standing voltage across the switching power devices

the capacitor's voltage as shown in Fig.5 (a and b). Through this, it can see the triple reinforcement of the input source, as well as the stability in the voltages of the capacitors, which is one of the most important advantages of the work of this inverter.

The three firing angles ($\alpha_1,\alpha_2,\alpha_3$) help to significantly reduce the THD as shown in Fig. 5(c,d) where we notice that the value of the total harmonic distortion has improved from**(18,31% to 15.32%)** as a result of the optimization technique used to implement the GAs optimized selective harmonic elimination.

The voltage stress of each switch in the tippler section (S_1, S_1', S_2, and S_2') was 100V. and their remaining polarity section (**S_3, S_3', S_4,** and **S4'**) is 300 volts, Fig .5.(e) shows the stress voltage across switches **S_1** and **S_3**.
These results confirm the mathematical analysis in the fourth section when comparing the proposed inverter with other studies, through which it was proved that the total standing voltage is equal to (16Vd.c).

Conclusions

This paper introduces a new inverter with seven levels with reduce all components of the inverter circuit. Eight switches, two diodes, two capacitors, and a single DC source make up the topology that was designed. Simple design work is produced by the output voltage's symmetrical upper and lower halves. the voltage gain Triple the input. Three firing angles were obtained using the SHE with GAs to reduce the lower order harmonics, which lower the THD value. Due to the proposed topology's ability to self-balance, the voltages of the capacitors are naturally balanced. The capacitor's voltages are maintained using a straightforward series-parallel method without any additional circuit or any sensors. The principle of operation and the simple pulse modulation method were discussed. The results of comprehensive and detailed studies are presented, and the operability and viability of the suggested topology are validated. Finally, A detailed comparison with the other operating topologies in terms of decreased components confirms the merits of the suggested topology.
It can be used as another optimization technique to improve THD and replace the D.C source with photovoltaic (PV) modeling in future works.

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