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Simulation Action Potential Signal Based On FPGA

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Abstract

This paper aim to generate and take Action potential signal (AP) then converts it to digital signal based on one bit Sigma-Delta converter (∑-Δ) to produce a 1-bit stream represent this signal with resolution of 10 bit. This data has been stored in proposed memory created in electronic device called Field Programmable Gate Array (FPGA) by which also the proposed converter had been designed and implemented practically. Finally, the obtained results analyzed and compared with other converter techniques to show the difference in the results and performance.
Keywords: Action potential; Sigma-Delta Converter; FBGA.

1. Introduction

The rapid and great development of the electronics industry has led to the ease of design and manufacture of electronic circuits, which in turn carry out electronic operations more accurate , high flexible and a few errors especially programmable electronic circuits such as Arduino, PLC, FPGA and etc[1]. This allows us to design and build any electronic circuit easily and without any complexity, which reduces the cost of manufacturing and the power consumption, in addition reducing the error rate in the circuit and also allows us to change the design at any time without the need to install new elements into this circuit[2]. Aim of this work is to generate and convert analog signal to digital signal and process it. The signal that had been processed in this paper is biological signal called Action Potential signal(APS). This signal had been converted by using Sigma-Delta analog to digital converter (Δ-∑ ADC) which designed based on Field Programmable Gate Array (FPGA) to decrease hardware and cost.

1.1 Action Potential Signal(APS)

The brain control on the organs using nerves connected to it as a complex network, where the brain send orders to the members depending on electric signals produced chemically, this signals called action potential signals (APS). To simulate this signal and deal with, we must know its behavior. Figure 1 illustrate the Approximate shape of action potential signal, when the neuron is stimulated to the threshold level the signal will be upraised to peak value at 40mv with time 2ms and then falls to -90 at time 3ms[3]. We note from the curve the signal carry on exponentially.

1.2 First Order Sigma-Delta Analog to Digital Converter(∑-Δ)

First Order Sigma-Delta Analog to Digital Converter(∑-ΔADC) convert analog signal to one bit stream digital signal, this property make the system simple and reduce the complexity as well as hardware[4]. The most important feature in this converter is it use very high sampling rate.

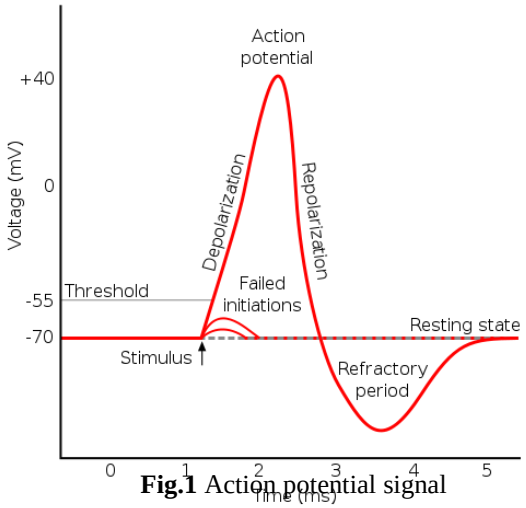

Fig.1 Action potential signal

The use very high sampling ratio has several benefits summarized below[5]:

- No strict requirements obligatory on analog building blocks.
- Low cost, low power consumption in digital filtering.
- Reduced baseband quantization noise power.
- High resolution of the digital output and better noise shaping.

The Sigma-Delta converter consist of a summer, an integrator, a comparator, a D flip-flop and a DAC as shown in the figure 2, the output of the converter is 1-bit stream converted by 1-bit digital to analog converter then fed back to compare it again with input signal[6].

1.2.1 Sigma-Delta Converter Verification

To verify the converter we had been designed it using Matlab/Simulink. Figure 3 illustrate the block diagram of

the system, figure 4 contain multi outputs represent the stages of signal passing through the converter ,

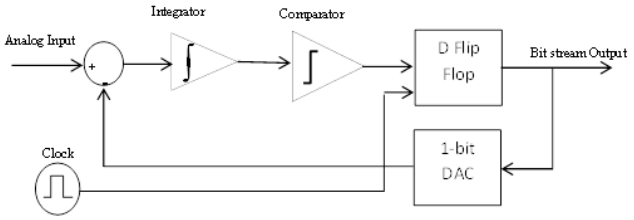

Fig. 2 Sigma-Delta Analog to Digital converter

The signal that used in verification is sinusoidal, we note from the figure the input wave compared with feedback signal which regard analog signal converted from digital output then integrated and quantized to several level to obtain proper resolution, this signal translated to a group of ones and zeros.

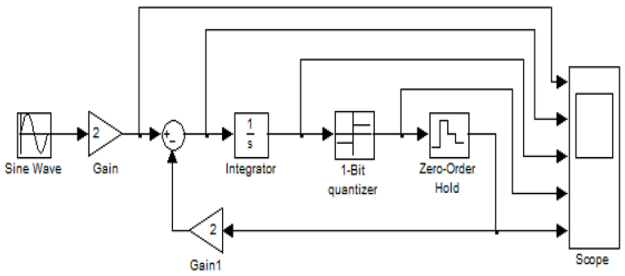

Fig. 3 Sigma-Delta Analog to Digital converter representation in Matlab/simulink

2. Hardware Implementation

The system consist of (APS) generated according eq. 1 in the programmable electronic device called FBGA then converted to digital signal by input it to 1-bit Sigma-Delta converter instead of use multi bit converters to reduce the hardware and quantization noise also power consumption in this case we use 10 bit resolution after this stage the signal converted to analog using Low Pass Filter (LPF) with attenuator resistance. Figure 5 illustrate the block diagram of the whole system.

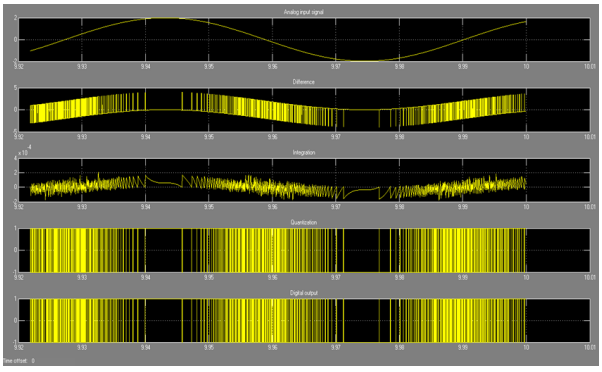

Fig. 4 Output of verification system

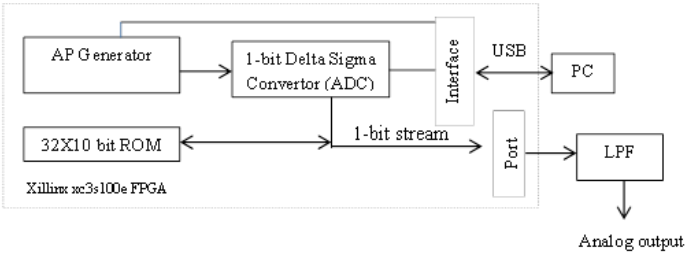

Fig.5 Block Diagram of the system

2.1 FPGA Unit

Digital FPGA structure offer a important speedup and real time signals over software designs, also size, weight, and power consumption efficiency. Compared to analog devices, digital FPGAs designs are stable and flexible in design alterations[7].

2.2 Low Pass Filter

The final stage of the system is the LPF that converts the digital signal to an analogue signal, figure 6 shows the attenuator and the RC filter to decrease the magnitude of high frequency[8].

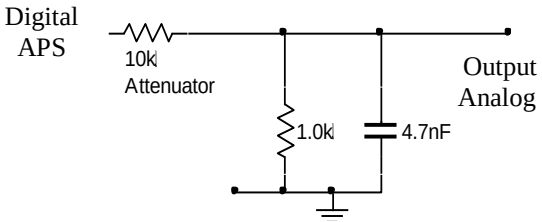

Fig.6 LPF Attenuator

3. Experimental results

APS signal is produced practically by built in designed generator in the FPGA as shown in the figure 7 according to the equation[8]:

$$v_m(t) = \begin{cases} At^n e^{-Bt} & t \geq 0 \\ 0 & t < 0 \end{cases} \dots\dots\dots\dots\dots\dots (1)$$

Where A and B are constants and n is an integer and its typical value is:
A=3.7*10-3Vs-1 , B= 1.5*104s-1 and n=1.

The magnitude of A,B and n can be changed to obtain waveform with specific options. This property increase the flexibility of the system where we can make the signal easier and faster without need to change or modify the software code or the hardware design. APS signal sampled where its duration is 0.64ms with 32 sample according sample frequency 48.828k sample/s as shown in the figure

8, each sample is represented by 10-bit binary number covering integer and decimal parts in it(show table 1) to make the conversion more precise and decrease the loss in the signal as well as decrease the ripple. Data conversion to binary require convert the integer and decimal part of the sample value, in this work we take three digit after point and make conversion by fixed point method using MATLAB code.

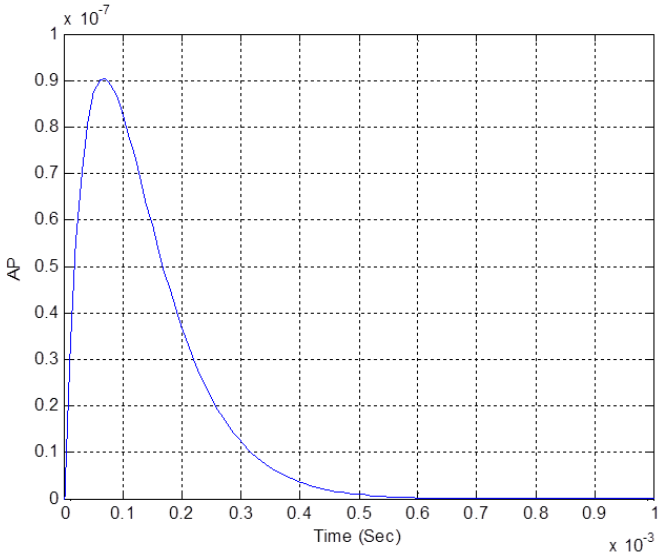

Fig.7 Output of the verification system

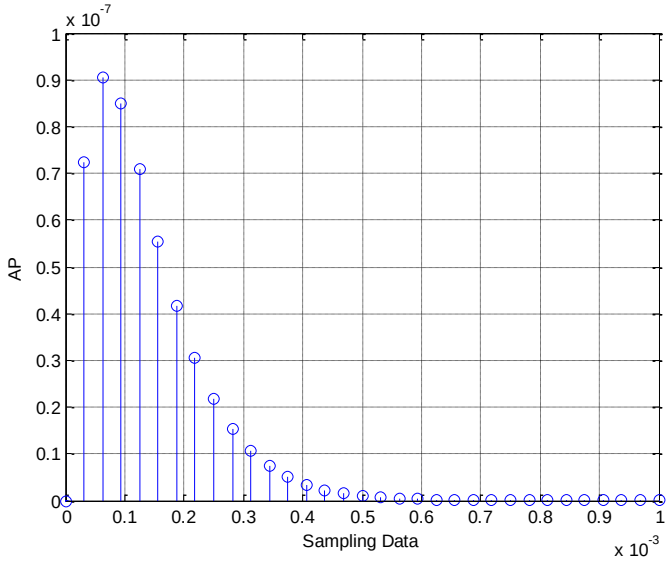

Fig.8 Sampled AP signal

In table 1 some samples had been taken to show the procedure by which the conversion done where the actual signal value processed to obtain fixed point value, this is rounded to the nearest integer value after this stage the signal is converted to digital (Hexa) to dealwith it.

Figure 9 shows the APS signal obtained practically using FPGA with 200µs/div horizontally and 500mv/div vertically.

The on-board 50 MHz clock is used as the timing reference for the Sigma-Delta converter generator. For the required 10 bit data precision, the Sigma-Delta converter sample rate is kept at just under 50kHz (48.8kHz to be exact) which is adequate for the generation of APS.

Table 1 illustrate some samples values of the signal

No.	Actual Value (mv)	Fixed point Value	Rounded value	Hexa Value
1	0.1785601	178.5601	179	B3
2	0.2989427	298.9427	299	12B
3	0.0712363	71.2363	71	047
4	0.0366962	36.6962	73	025
5	0.0042040	4.2040	4	004
6	0.001970	1.9707	2	002

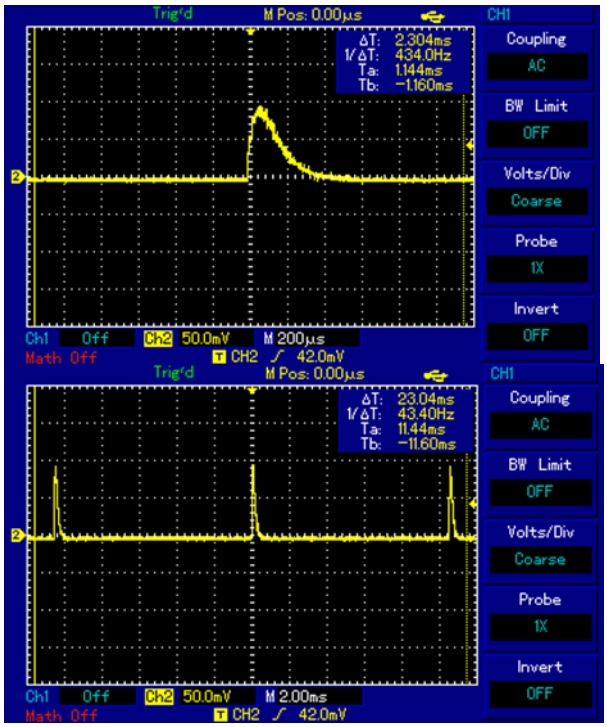

Fig.9 AP signal obtained practically

The overall system takes up only 35% of the available FPGA slices and total CPU time to Xst completion: 0.36 secs, as illustrated in the table 2 thereby suggesting that further savings could be achieved if the design was implemented on a custom circuit board.

3.1 Case study 1: Analog to digital converter design by Pulse Width Modulation (PWM) instead of sigma-delta method.

A.Al-Shueli,and C.T. Clark[9] had been designed Analog to digital converter using FPGA but by using Pulse Width Modulation (PWM) technique, where we see the total used

memory 38% compared with our work that use 35% also the power consumption using Sigma-Delta is 15.98mW while by using PWM became22.56mW. Table 3 shows the comparison between utilization of Common components in FPGA using Sigma-Delta and PWM technique, where we note that the number of used component by PWM method is more than Sigma-Delta method this lead to use high size memory as well as there is saving in the power due to using the second method.

Table 2 illustrates FPGA utilization summary

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	36	1,920	1%	
Number of 4 input LUTs	658	1,920	34%	
Number of occupied Slices	343	960	35%	
Number of Slices containing only related logic	343	343	100%	
Number of Slices containing unrelated logic	0	343	0%	
Total Number of 4 input LUTs	676	1,920	35%	
Number used as logic	33			
Number used as a route-thru	18			
Number used as Shift registers	625			
Number of bonded IOBs	7	83	8%	
IOB Flip Flops	1			
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	1.31			

Table 3 shows the comparison between utilization of Common components FPGA using Delta-Sigma and PWM technique

No.	Item	Used		Available	Utilization (%)	
		Δ-∑	PWM		Δ-∑	PWM
1	Number of slice flip flop	36	45	1920	1%	2%
2	Number of 4 inputs LUTS	658	726	1920	34 %	37
3	Number of occupied slices	343	380	960	35 %	39
4	Number used as logic	33	101			
5	Number used as shift register	625	625			
6	Number of bonded IOBs	7	8	83	8%	9%
7	Memory used	35%	38%			
8	Power consumption	15.98m W	22.56m W			

3.2 Case study 2: Design Sigma-Delta ADC by Microcontroller instead of FPGA.

Anju Ashok, Anusha Zachariah[10] had been designed Sigma-Delta ADC by microcontroller. In this method we note the design of converter pass through four stage (Coding , Compiling, Simulation, and Burning), these stage require external hardware implementation and additional programs while FPGA outline all this stage in it without need to external devices (complexity less) as well as FBGA run the conversion faster compared with microcontroller. Also the power consumption in FBGA regard few compared with microcontroller.

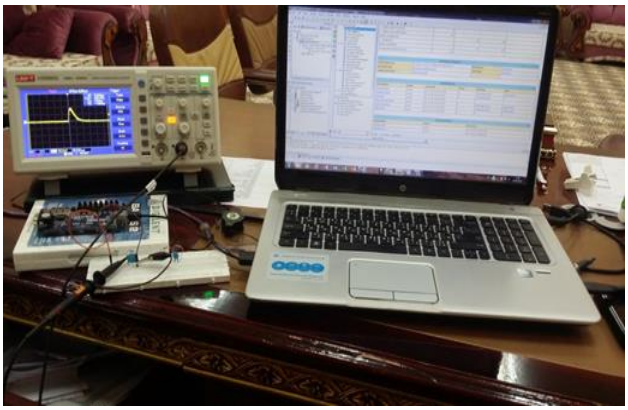

Fig.10 Delta Sigma converter implementation

Mem[0] =12'h000	Mem[8]=12'h0C0	Mem[16]=12'h026	Mem[24]=12'h006
Mem[1] =12'h0B7	Mem[9]=12'h0A1	Mem[17]=12'h01E	Mem[25]=12'h004
Mem[2] =12'h112	Mem[10]=12'h086	Mem[18]=12'h018	Mem[26]=12'h003
Mem[3] =12'h133	Mem[11]=12'h06E	Mem[19]=12'h013	Mem[27]=12'h003
Mem[4] =12'h132	Mem[12]=12'h05A	Mem[20]=12'h00F	Mem[28]=12'h002
Mem[5] =12'h11E	Mem[13]=12'h049	Mem[21]=12'h00C	Mem[29]=12'h002
Mem[6] =12'h101	Mem[14]=12'h03B	Mem[22]=12'h009	Mem[30]=12'h001
Mem[7]=12'h0E0	Mem[15]=12'h02F	Mem[23]=12'h007	Mem[31]=12'h001

Table 4 illustrate Peak Memory Usage: 159 MB

4. Conclusion

In this paper, first order Sigma-Delta analog to digital converter is designed and implemented practically on FPGA, LPF and attenuator. Action potential signal is taken and converted to 1-bit stream digital signal with 10 bit to increase the resolution. The results obtained were compared with other results got from the use of different methods, whether different devices like micro controller or techniques used like PWM, where it provide a abbreviation in the hardware implementation and power consumption as well as decrease the complexity of the circuit.

5. References

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